A *W*-Band Image-Rejection Downconverter

Kwo Wei Chang, Huei Wang, *Member, IEEE,* Thuy-Nhung Ton, *Member, IEEE,*
Tzu-hung Chen, *Member, IEEE,* Kin L. Tan, *Member, IEEE,* Gee Samuel Dow,
G. M. Hayashibara, Barry R. Allen, *Member, IEEE,* John Berenz,
Po-Hsin Liu, Dwight C. Streit, and Louis C. T. Liu, *Member, IEEE*

Abstract—**This paper presents the design, fabrication, and evaluation of a *W*-band image-rejection downconverter based on pseudomorphic InGaAs/GaAs HEMT technology. The image-rejection downconverter consists of a monolithic three-stage low-noise amplifier, a monolithic image-rejection mixer, and a hybrid IF 90° coupler with an IF amplifier. The three-stage amplifier has a measured noise figure of 3.5 dB with an associated small signal gain of 21 dB at 94 GHz while the image-rejection mixer has a measured conversion loss of 11 dB with a +10 dBm LO drive at 94.15 GHz. Measured results of the complete image-rejection downconverter including the hybrid IF 90° coupler and a 10 dB gain IF amplifier show a conversion gain of more than 18 dB and a noise figure of 4.6 dB at around 94 GHz.**

I. Introduction

The *W*-band downconverter is a key component for smart munitions and millimeter-wave imaging applications. A fully integrated pseudomorphic (PM) InGaAs/GaAs HEMT downconverter MMIC, which consists of a two-stage low-noise amplifier and a single-balanced diode mixer, has been successfully developed recently [1]. The complete monolithic downconverter exhibited 5.5 dB conversion gain and 6.7 dB double side-band (DSB) noise figure with a 95 GHz LO and a 1 GHz IF. Although this monolithic downconverter has shown good performance at *W*-band and represents state-of-the-art in millimeter-wave monolithic device and circuit technology, insertion of the *W*-band MMIC into existing systems and evolution of new system applications rely on further improvement of the downconverter performance. The intention of this work is to explore the feasibility of improving the noise figure and conversion gain of the existing monolithic downconverter.

A *W*-band image-rejection (IR) downconverter based on 0.1 μm PM InGaAs/GaAs HEMT technology has been developed. The IR downconverter consists of a monolithic three-stage low-noise amplifier, a monolithic image-rejection mixer (IRM), and a hybrid IF 90° coupler with an IF amplifier. The three-stage LNA improves the overall system sensitivity while the IRM receives signals at frequencies either lower or higher than the LO frequency and allows suppression of image signals. Moreover, the IRM eliminates the need of a preselect image suppression filter, which is difficult to realize for a low IF frequency *W*-band receiver. The IRM consists of two single-balanced (SB) mixers which were designed using the HEMT gate Schottky diodes inherent to the process and can be integrated monolithically with the LNA. The three-stage amplifier has a measured noise figure of 3.5 dB with an associated small signal gain of 21 dB at around 94 GHz while the IRM has a measured conversion loss of 11 dB with only 10 dBm LO drive. The IRM provides more than 12 dB rejection at the image frequency with a hybrid IF 90° coupler. Measured results of the complete downconverter including the hybrid IF 90° coupler and a 10 dB gain amplifier show a conversion gain of more than 18 dB and a noise figure of 4.6 dB at around 94 GHz. This is the best reported performance of a *W*-band downconverter and shows significant improvement compared with previously reported results in terms of noise figure and conversion gain. The success of this image-rejection downconverter development is attributed to the excellent device performance and a rigorous design/analysis methodology. This state-of-the-art performance shows the potential of the emerging technology for low cost *W*-band receiver applications.

The PM InGaAs/GaAs HEMT device characteristics are described in Section II and the MMIC circuit design and fabrication are presented in Sections III and IV, respectively. Section V summarizes the circuit performance and is followed by a conclusion.

II. Device Characteristics and Modeling

The devices reported in this paper have been optimized for high gain operation at *W*-band. The 22% PM InGaAs HEMT uses planar doping to achieve high channel aspect ratio as well as higher electron transfer efficiency. A cross-section and a SEM photograph for the gate area of the HEMT device are shown in Fig. 1(a) and (b). The 0.1 μm T-gate PM InGaAs HEMTs fabricated using this process typically have a dc transconductance (G_m) of 670 mS/mm with a cutoff frequency (f_T) as high as 140 GHz. The discrete HEMT device dc yield in process control monitors (PCMs) on the 3″ diameter GaAs wafer is 83%. This process has demonstrated excellent yield and reproducibility over the past two years and is presently transferred to production in our manufacturing process line.

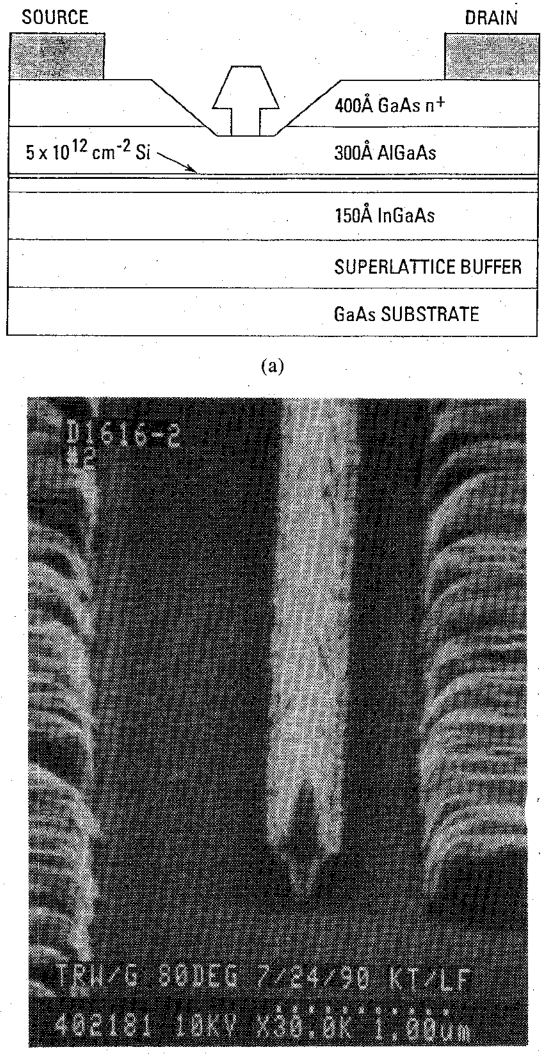
The HEMT linear small-signal equivalent circuit parameters are obtained by carefully fitting the measured

---

Manuscript received March 31, 1992; revised July 27, 1992.

The authors are with TRW/ESG, Electronics and Technology Division, One Space Park, Redondo Beach, CA 90278.

IEEE Log Number 9203699.



(a)

(b)

Fig. 1. (a). The profile and (b) the SEM photograph for the gate area of a 0.1 μm PM InGaAs/GaAs HEMT device.

small-signal S-parameters to 40 GHz. Noise model parameters used for the simulation are obtained from fitting measured noise parameters to 26 GHz. The small signal equivalent circuit and noise model of a 40 μm HEMT biased at peak transconductance and 2 V drain voltage was reported in [3]. These parameters are consistent with estimations based on device physical dimensions and parameters. A set of specifically designed on-wafer calibration standards consisting of co-planar wave-guide (CPW) open, short, load and through patterns which have the same feed patterns as the device to be tested are modeled carefully via a full-wave EM analysis [2]. The measurement accuracy can be ensured by using these calibration patterns, thus improving the accuracy of the frequency extrapolation model to W-band. The details of this modeling procedure was documented in [3].

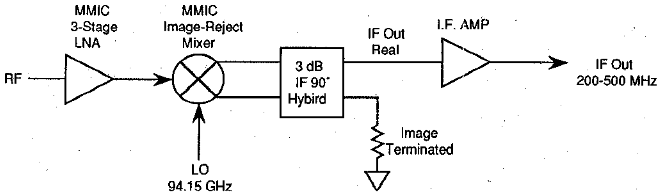
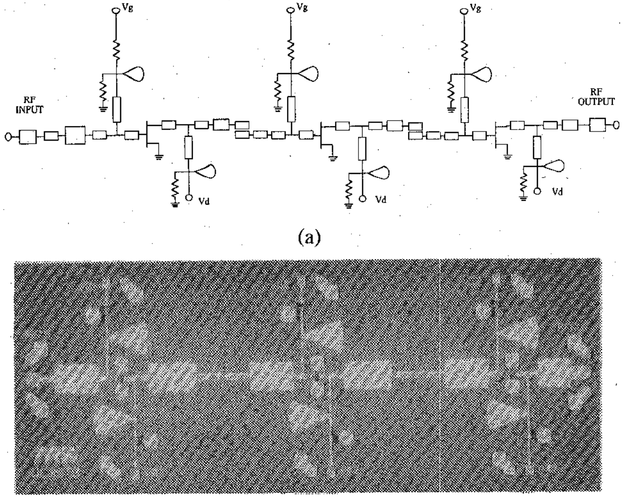


Fig. 2. Simplified block diagram of image-rejection downconverter.



(a)

(b)

Fig. 3. (a) Circuit schematic and (b) Photograph of three-stage LNA.

III. Circuit Design

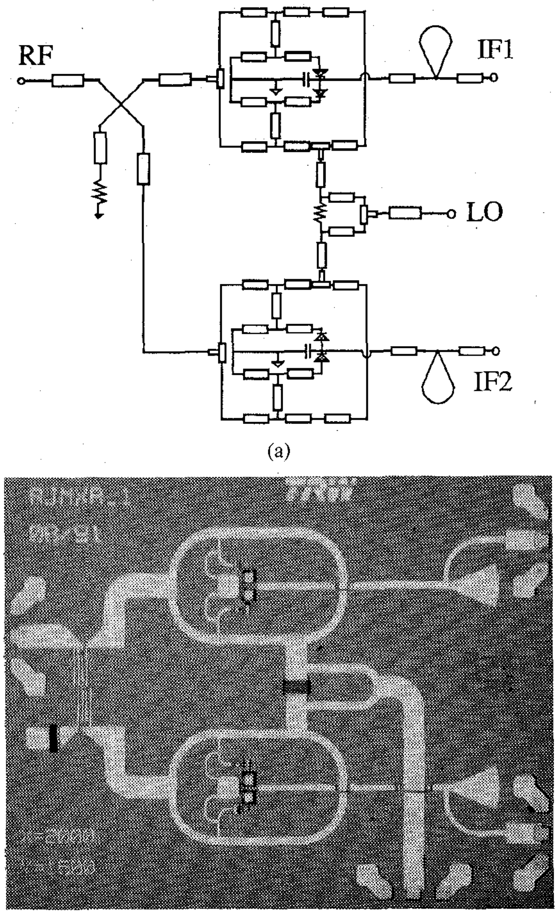
Fig. 2 illustrates the block diagram of image-rejection downconverter. It consists of a three-stage LNA, an IRM, a hybrid IF 90° coupler, and an IF amplifier. The LNA and IRM are monolithic MMICs whereas the IF 90° coupler and IF amplifier are off-the-shelf components. The following describes the design of LNA, IRM and downconverter circuits.

Low-Noise Amplifier

Fig. 3(a) and (b) show a circuit schematic and photograph of the monolithic three-stage LNA. The chip size is 3.2×1.2 mm^2. It is a single-ended design and each stage utilizes a 40 μm HEMT with four gate fingers. The circuit is designed for low noise figure based on a reactive matching technique. The matching networks are quasi-low pass filter structures and realized by cascade high-low impedance microstrip lines on 100 μm thick GaAs substrate. Edge-coupled lines are used for dc blocking and radial stubs are employed for RF by pass. N$^+$ bulk resistors are used to ensure bias network stability, and a reactive ion etching (RIE) process is used to fabricate back side via holes for the RF grounding. Details of the design methodology were described in [3].

Image-Rejection Mixer

Fig. 4(a) and (b) show a circuit schematic and photograph of the monolithic IRM. The chip size is 2.1×1.6 mm^2. The IRM was realized with two single-balanced diode mixers, a W-band Lange coupler, and a Wilkinson power divider. The RF and LO signals are fed in quadrature and in phase, respectively, to the mixer. The Lange



(a)

(b)

Fig. 4. (a) Circuit schematic and (b) Photograph of image-rejection mixer.

coupler is used for the RF port to achieve a better input return loss.

The single-balanced mixer is the key element of the IRM and was designed with a 180° rat-race hybrid for the RF and LO signal inputs and a matched pair of 16 μm InGaAs/GaAs HEMT gate Schottky diodes for the mixing elements. In order to minimize the mixer size, the diodes are positioned inside the ring and both the MIM capacitor and shunt radial stubs are used to realize the IF low pass filter. The low pass filter provides a short for RF and LO frequencies at the mixer output port. The diode matching circuits are realized with high impedance microstrip lines and provide the path for diode dc return. No dc bias is included for the current mixer circuit although a dc bias may be added to reduce the required LO power for the same conversion loss. The diode structure and model were reported in [1].

Image-Rejection Downconverter

The *W*-band IR downconverter is built with two MMIC chips mounted on a test fixture and combined externally with a 200–500 MHz hybrid IF 90° 3-dB coupler. Since the RF signals are 90° out of phase and the LO inputs are in phase, the upper and lower IF mixing sideband are separated at the two output ports of the IF 90° hybrid. The desired sideband is fed to a 10 dB IF amplifier while the image sideband is terminated at a resistive load. The principle of an IR mixer is explained in [4].

IV. CIRCUIT FABRICATION

Both LNA and IRM MMIC chips were fabricated on an InGaAs/GaAs heterostructure HEMT wafer. The MMIC process is similar to that previously reported [5], [6], it begins with multiple oxygen implantations to obtain a device isolation of better than 10^7 ohms. Ohmic contacts are deposited using a Ni/AuGe/Ag/Au evaporation and lift-off process, and are alloyed using a rapid thermal anneal at 540°C. The 0.1 μm Ti/Pt/Au T-gate defined using a Philips EBPG-3 electron-beam lithography system with a two-layer PMMA/P(MMA-MAA) resist. Discrete device yields are typically greater than 80% using this T-gate process. A thin layer of metal (Ti-Au) is deposited and lifted-off to form the low resistance first level metal interconnects. The airbridge and transmission lines consist of 2 μm of Ti/Au. Via holes with a diameter of 60 μm were etched through the 100-μm thick GaAs substrate using RIE to provide low source grounding inductance.

V. CIRCUIT PERFORMANCE

The amplifier, mixer, and IR downconverter have been tested in waveguide test fixtures. Finline transitions are used to couple the *W*-band signals from waveguide to microstrip. The insertion loss of two transitions (back to back) is about 1.4–2.0 dB for 88–96 GHz frequency range. All the measurement data described below has been corrected for the RF and LO transition losses.

Low-Noise Amplifier

The measurement data from 91–97 GHz is presented in Figure 5. The noise figure is better than 4 dB and the associated small signal gain is greater than 20 dB across the band. At 94 GHz, the amplifier demonstrates 21 dB gain with a 3.5 dB noise figure. The noise and gain variation are within 0.5 and 2 dB, respectively, across the band. The data was taken with a drain voltage of 2.5 V and a gate voltage of 0 V for each stage. Other chips on the wafer showed similar performance. The improvement of noise performance compared to previously published results [3], [7] is due to the improved noise match.

Image-Rejection Mixer

Before testing the IR mixer, the performance of the SB mixer used in the IR mixer was verified. Fig. 6 illustrates the measured and simulated mixer conversion loss as a function of the LO power. The RF and LO frequencies are fixed at 96 and 96.25 GHz, respectively. The conversion loss is about 9.5 dB when LO power is greater than 7 dBm and remains almost unchanged for greater LO powers. The agreement between the measured and simulated results is within 2 dB for LO powers greater than 3 dBm.

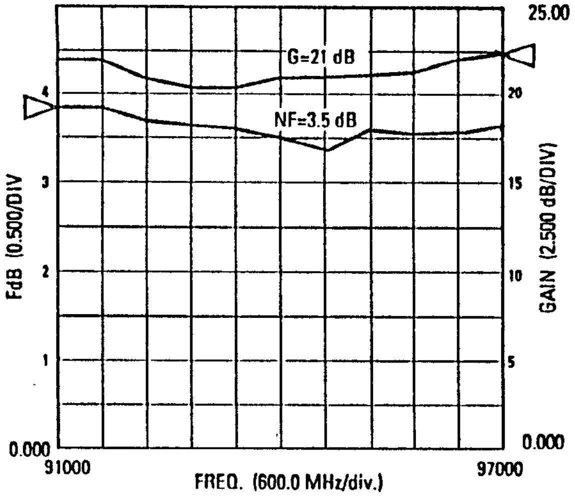


Fig. 5. Measured noise figure and associated small-signal gain *W*-band three-stage MMIC LNA from 91-97 GHz.

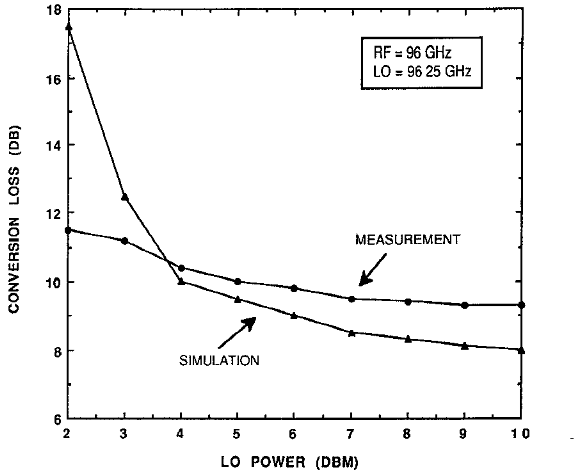
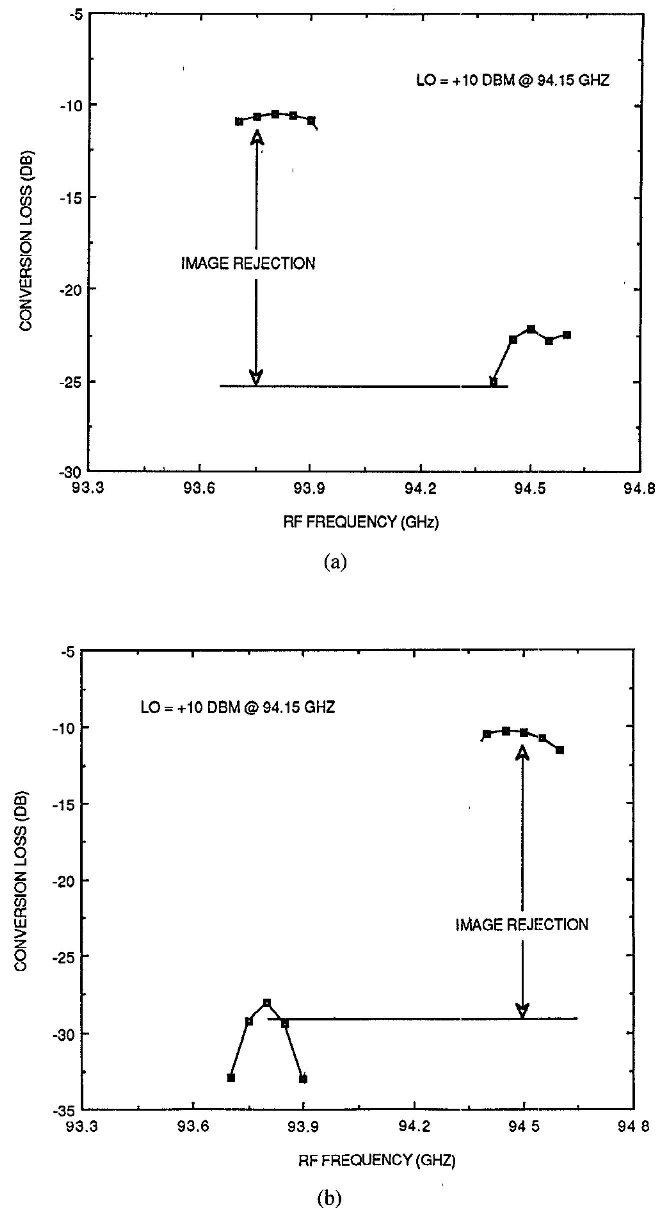


Fig. 6. Measured and simulated conversion loss of the single-balanced mixer as a function of the LO power. The RF and LO frequencies are 96 GHz and 96.25 GHz, respectively.

The IR mixer MMIC was mounted on a fixture and tested with a NARDA 200-400 MHz hybrid 90° 3-dB coupler connecting to its two output ports. To test the level of image rejection, one of the coupler outputs (for example, the Q-port in Fig. 2) is terminated with 50-ohm resistor and the conversion loss from the mixer input to I-port output is measured for both lower sideband (LSB) and upper sideband (USB) RF frequencies. The image rejection for I-port is calculated as the difference of the conversion losses for LSB and USB. The Q-port image rejection is also measured with the I-port terminated with 50-ohm. Fig. 7(a) and (b) show the measured conversion loss and image rejection for I-port and Q-port, respectively, for a +10 dBm LO power at 94.15 GHz. The conversion loss is approximately 11 dB for both I-port and Q-port whereas the image rejection is in general higher for the Q-port. The actual image rejection is dependent upon the IF frequency.



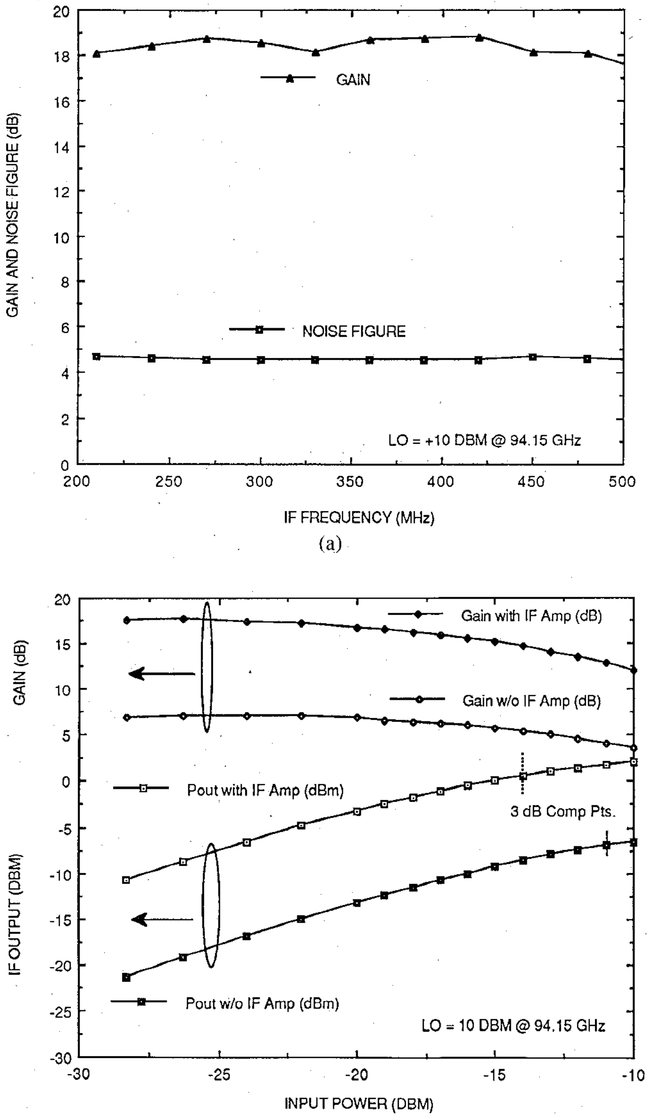
(a)

(b)

Fig. 7. Measured conversion loss and image-rejection of the (a) I-port and (b) Q-port IF outputs. A NARDA 215-450 MHz 90° hybrid was used to combine the two mixer outputs.

Image-Rejection Downconverter

The three-stage LNA, IR mixer, hybrid IF 90° coupler, and a 10 dB gain IF amplifier were assembled together to build the IR downconverter. Fig. 8(a) shows the measured noise figure and gain of the downconverter for IF frequency between 200 MHz and 500 MHz. The LO power is +10 dBm at a fixed frequency of 94.15 GHz. The gate and drain for the LNA are biased at zero and three volts, respectively. The downconverter has less than 4.6 dB noise figure and more than 18 dB conversion gain across the IF bandwidth. The measured compression characteristic of the IR downconverter is plotted in Fig. 8(b). The calculated output 3 dB compression point is about −2 dBm. This is the best noise figure reported to date for a *W*-band monolithic front end IR downconverter.



(a)

(b)

Fig. 8. Measured (a) noise figure and associated conversion gain and (b) compression characteristic of IR downconverter. The IR downconverter consists of the monolithic LNA and IR mixer chips, a NARDA 215-450 MHz 90° hybrid, and a NEC UPG100B amplifier.

VI. CONCLUSION

A *W*-band image-rejection downconverter based on PM InGaAs/GaAs HEMT device technology has been designed, built and tested. This downconverter integrates a three-stage MMIC LNA, an IR MMIC mixer, a hybrid IF 90° coupler, and an IF amplifier into one unit. Measured results of the complete downconverter show a conversion gain of greater than 18 dB and a noise figure of less than 4.6 dB around 94 GHz. This is the best reported performance of a *W*-band downconverter and shows significant improvement compared with previously reported results in terms of noise figure and conversion gain. The success of this image-rejection downconverter development is attributed to the excellent device performance and a rigorous design/analysis methodology. Furthermore, this state-of-the-art performance shows the potential of MMIC insertions into low cost *W*-band receiver applications.

ACKNOWLEDGMENT

The authors would like to thank J. Coakley and J. Yonaki for the layout effort, J. J. Raggio for the device testing, R. Dia for wafer processing, the MBE and EBL groups in TRW for their excellent help and MIMIC Phase 2 Program for the support of chip testing. The authors also acknowledge L. Wiederspahn for his helpful discussions and suggestions.

REFERENCES

[1] K. W. Chang, *et al.*, "A *W*-band monolithic downconverter," *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 12, pp. 1972-1979, Dec. 1991.

[2] J. C. Rautio and R. F. Harrington, "An electromagnetic time-harmonic analysis of shielded microstrip circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 35, pp. 726-730, Aug. 1987.

[3] H. Wang *et al.*, "High performance *W*-band monolithic InGaAs pseudomorphic HEMT LNAs and design/analysis methodology," *IEEE Trans. Microwave Theory Tech*, vol. 40, no. 3, pp. 417-428, Mar. 1992.

[4] S. A. Maas, *Microwave Mixers*. Norwood, MA: Artech House, 1986.

[5] K. L. Tan *et al.*, "94 GHz 0.1 μm T-gate low-noise pseudomorphic InGaAs HEMTs," *IEEE Electron Device Lett.*, vol. 11, no. 12, pp. 585-587, 1990.

[6] M. V. Aust, *et al.*, "A family of InGaAs/AlGaAs V-band monolithic HEMT LNA's," in *1989 IEEE GaAs IC Symp. Dig.*, pp. 95-98, Nov. 1989.

[7] H. Wang *et al.*, "State-of-the-art low noise performance of 94 GHz monolithic amplifiers using 0.1 μm InGaAs/GaAs pseudomorphic HEMT technology," in *IEEE Int. Electronic Device Meeting Dig.* Washington, D.C., Dec., 1991, pp. 939-942.

Kwo Wei Chang received the B.S. degree in electrophysics from the National Chiao-Tung University, Taiwan, in 1977 and the M.S. and Ph.D. degrees in electrical engineering from SUNY, Stony Brook, NY, in 1981 and 1985, respectively. His graduate study involved in the research of SAW and magnetostatic wave devices for microwave applications.

From 1985 to 1989, he was a member of Technical Staff in the microwave receiver group of David Sarnoff Research Center, Princeton, NJ where he was responsible for the design and development of receiver components and systems. He also worked on the electronically steerable flat antenna for DBS applications. Dr. Chang joined TRW in December 1989. He is currently an Engineer of the Communication Systems Development Department and is interested in the nonlinear microwave and millimeter wave circuits and nonlinear device modeling.

Huei Wang (S'83-M'87) was born in Tainan, Taiwan, Republic of China on March 9, 1958. He received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, Republic of China in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Michigan State University, East Lansing, in 1984 and 1987, respectively.

During his graduate study, he was engaged in the research on theoretical and numerical analysis of electromagnetic radiation and scattering problems. He was also involved in the development of microwave remote detecting/sensing systems. He has been with the Electronics and Technology Division of TRW, Inc. since 1987, where he has been responsible for MMIC modeling of CAD tools, MMIC testing and evaluation. He is currently in charge of the development for monolithic millimeter-wave integrated circuits and subsystems.

Dr. Wang is a member of Tau Beta Pi and Phi Kappa Phi.

Thuy-Nhung Ton (M'86) received the B.S.E.E. degree from the University of California, Irvine in 1983.

In 1983, she joined Microwave Product Division, Hughes Aircraft Company as a member of the Technical Staff where she was involved with the analysis, design, fabrication, and characterization of millimeter-wave components and subsystems. Since 1987, she has been with Microwave Technology and Development Operation of the Electronics and Technology Division of TRW. She is responsible for the design and development of microwave and millimeter-wave MMIC's using MESFET and HEMT technologies. In addition, she is investigating the packaging techniques for module integration using MMIC's.

Ms. Ton has published several papers on millimeter-wave integrated CPW receivers, high dynamic range mixers, and filters.

Tzu-hung Chen (S'83–M'84) was born in Taiwan, R.O.C. on May 17, 1954. He received the B.Ed. degree in physics from National Changhwa University in 1972, the M.S. degree in physics from National Taiwan Normal University in 1978, and the Ph.D. degree in electrical engineering from University of Minnesota in 1984.

From 1984 to 1986 he was with GE, Syracuse, NY, working on the MMIC design and device modeling of MESFET and HEMT. From 1986 to 1988 he was a Senior Engineer in Microwave Semiconductor Corp., Somerset, NJ, where he worked on MMIC design and device modeling and characterization. In 1988 he joined the Electronics Technology Division, TRW, Redondo Beach, CA, where he is a Staff Engineer working on the nonlinear device modeling and monolithic microwave and wave integrated circuit design.

Kin L. Tan (M'90) received the B.S. and M.S. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 1983 and 1985, respectively.

In 1985, he joined Honeywell Physical Sciences Center in Bloomington, MN, where he worked on device development and process integration for submicron high speed GaAs Digital MESFET IC's. In 1989, he joined Hughes Microwave Products Division, Torrance, CA, where he was involved in the development of high efficiency power MESFET's and HBT's for microwave applications. Since 1990, he has been with the Advanced Microelectronics Laboratory, TRW Electronics Technology Division, Redondo Beach, CA, where he currently is Section Manager of HEMT product engineering, working on low noise and power millimeter-wave HEMT devices and MMIC's.

Gee Samuel Dow (S'78–M'82) was born in Tainan, Taiwan on April 12, 1954. He received the diploma in electrical engineering from Taipei Institute of Technology, Taipei, Taiwan in 1974 and the M.S.E.E. degree from University of Colorado, Boulder, in 1981.

From 1981 to 1983 he was with Microwave Semiconductor Corporation, where he worked on the development of *Ku*-, *K*-band MESFET power amplifiers and multipliers. From 1984 to 1987, he was with Hughes Aircraft Company, Microwave Products Division, where he was engaged in the characterization of power MESFET devices, development of wideband, high efficiency power amplifiers, and DRO's. Currently, he is with TRW Electronics Technology Division, where he manages a MMIC design section. During the past several years, this group has published extensively in the area of microwave and millimeter-wave monolithic circuits design up to 100 GHz.

Mr. Dow has authored and co-authored over 30 publications in the area of MIC/MMIC design.

Barry R. Allen (S'82–M'83) was born in Cadiz, KY, on November 5, 1947. He received the B.S. degree in physics and the M.S. and Sc.D degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1976, 1979, and 1984, respectively.

He joined TRW in 1983 as a Senior Staff member and has held a number of positions since then, including Section Head and Special Assistant for Technology. Since 1983 he has ben involved in all aspects of MMIC design and modelling, and is currently Assistant Program Manager for Design on the DARPA MIMIC Program. His main interests are low noise receiving systems, millimeter wave circuits, and accurate circuit modeling. Since 1985 he has been principle investigator for a GaAs MMIC IR&D project, which has resulted in several system insertions of MMIC. He was Program Manager of a millimeter-wave HEMT device and circuit development and has been involved in several other millimeter-wave development efforts. His current interests are accurate nonlinear models for improved distortion analysis of microwave and millimeter-wave circuits. From 1970 to 1975, he was with the Chesapeake and Potomac Telephone Company of Virginia working on microwave and radio telecommunications equipment. From 1975 to 1983, he was a member of the Research Laboratory of Electronics at MIT both as an undergraduate and as a Research Assistant in radio astronomy. While at MIT he was responsible for the development of low noise receiving systems spanning 300 MHz to 43 GHz.

In 1991, Dr. Allen became a TRW Technical Fellow in the Space and Defense Sector. He has published several papers on circuit applications of heterojunction devices and MMIC's. In 1990, he served on the Technical Program Committee for the IEEE MIT-S International Microwave Symposium.

John Berenz is a TRW Space & Defense Sector Technical Fellow and a Senior Scientist for the Electronics and Technology Division Microwave Technology and Development Operation. He has over 18 years experience in the design and fabrication of III-V semiconductor devices and integrated circuits. Before joining TRW in 1980 he was employed by Varian Associates and Hughes Aircraft Company.

Dr. Berenz has co-authored over 60 papers in this field.

Po-Hsin Liu received the B.S. degree in organo silicon chemistry from National Taiwan University, Taipei, Taiwan in 1969, and the M.S. and Ph.D. degrees in Physical and photo-chemistry from Washington University, St. Louis, MO in 1973 and 1975, respectively.

He is Manager of Advanced Electron-Beam Lithography Section for the Advanced Microelectronics Laboratory of TRW's Millimeter-Wave Technology and Development Operation. He has been the pioneer in electron-beam lithography at TRW since 1980. He has 15 years experience in the resist related fields and 10 years experience in direct-write electron-beam lithography.

Dr. Liu is author or co-author of over 20 technical papers.

Dwight C. Streit (S'81–S'85–M'85–M'86) received the Ph.D. degree in electrical engineering from UCLA in 1986.

He is currently manager of the GaAs Materials Section in TRW's Advanced Microelectronics Laboratory, where he is responsible for epitaxial material growth and III-V material analysis. His primary research interest is the relationship between material characteristics and device performance. His work has dealt with both HBT and HEMT material development and device design. Dr. Streit is a member of Tau Beta Pi, Eta Kappa Nu, and Sigma Xi.

Louis C. T. Liu (S'77–M'81) received the B.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1974 and the M.S. and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, in 1978 and 1981, respectively.

While at Cornell, he worked as a graduate research assistant in the field of microwave broad-band circuit synthesis and design with applications in both low-noise and high-power GaAs MESFET amplifiers, as well as monolithic microwave integrated circuits. In May 1981, he joined the Torrance Research Center of Hughes Aircraft Company, where he was responsible for the development of various monolithic low-noise and power amplifiers, as well as monolithic components for receive and T/R modules operating from *S*-band to *Ka*-band. In February 1986, Dr. Liu joined TRW. Currently, he is Assistant Manager of the Communication Systems Development Department and is responsible for the development of microwave and millimeter-wave monolithic amplifiers, mixers and phase shifters. He is also responsible for establishing the CAD methodology and workstation for MMIC designs.